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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,244	09/26/2003	Yoshihisa Dotta	1035-472	8593
23117	7590	10/05/2005	EXAMINER	
NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203			ANDUJAR, LEONARDO	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/670,244

Applicant(s)

DOTTA ET AL.

Examiner

Leonardo Andújar

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 July 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 3, 7, 11, 15, 16, 19-21, 23-25, 27 and 28 is/are allowed.
- 6) ☒ Claim(s) 1, 2, 5, 6, 9, 10, 13, 14, 17, 18 and 29 is/are rejected.
- 7) ☒ Claim(s) 4, 8, 12, 22 and 26 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07/13/2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Acknowledgment

1. The amendment filed on 07/13/2005 in response to the Office action mailed on 4/19/2005 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-29.

Election/Restrictions

2. Applicant's election without traverse of species 1 (claims 1-12) in the reply filed on 03/05/2005 is acknowledged. However, all claims were examined since the prior art make of record is pertinent to each of the claims.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

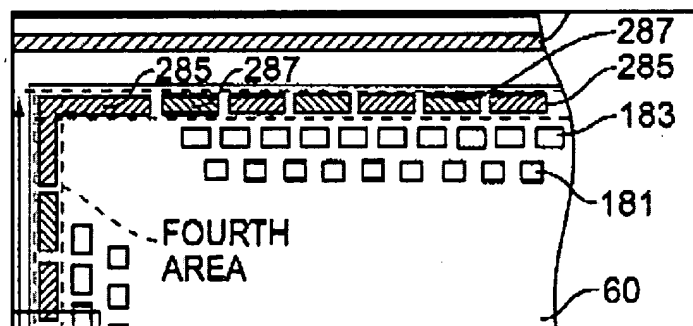
4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 2, 5, 6, 9, 10, 13, 14, 17, 18 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terui (US 006534879B2) in view of Gnadinger (US 005229647A).

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6. Regarding claims 1, 9 and 29, Terui (e.g. fig. 5A) shows a semiconductor device, comprising: a semiconductor chip 60, multiple electrodes (181, 183, 285, 287) formed on a front surface of the semiconductor chip wherein the multiple electrodes comprises a first electrode (181) and a second electrodes (183). The first and second electrodes have mutually differing cross-sectional areas in a common horizontal plane traversing the pad thickness (e.g., top surface). Also, the first and second electrodes have mutually differing resistance. Note that the resistance depend on the cross sectional area of the pad. Terui does not show that the electrodes are "through electrodes" linking the front surface and back surfaces of the chips.



Nevertheless, Gnadinger (e.g. fig. 4) shows through electrodes 20 linking front and back surfaces of the semiconductor chip 10/11. According to Gnadinger a very low cost high-density package can be obtained by using this type of through electrodes because this type of electrodes form reliable and inexpensive connections (col. 1/lls. 35-39 & 49-57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use through electrodes linking the front and back surface of Terui's chip to stack several chips in order to make a very low cost high density

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package as taught by Gnadinger because this type of through electrode forms reliable and inexpensive connections.

7. Regarding claim 2, Gnadinger shows that at least one type of the through electrodes is contact through electrodes electrically connected to the semiconductor chip (col. 2/lis. 6-21 & 49-62).

8. Regarding claim 9, Terui shows that cross sectional areas of the electrodes 285/287 connected to the power supply are greater than the cross sectional areas of those electrodes 181/183 which are connected to the signal terminal.

9. Regarding claims 13 and 14, Terui (e.g. fig. 5A) shows a semiconductor device, comprising multiple through electrodes (181, 183, 285, 287) formed on a front surface of a semiconductor chip 60 wherein the multiple electrodes comprises first electrodes (181) and second electrodes (183). The first and second electrodes have mutually differing cross-sectional areas in a common horizontal plane traversing the pad thickness (e.g., top surface). Also, the electrodes 181/183 is in contact electrically connected to the chip since they are signal terminals. Terui does not show that the chips are staked and that the electrodes are through electrodes linking the front surface and back surfaces of the chips. Nevertheless, Gnadinger (e.g. fig. 4) shows a device having stacked semiconductor chips having through electrodes 20 linking front and back surfaces of the semiconductor chip 11. According to Gnadinger a very low cost high-density package can be obtained by using this type of through electrodes because this type of electrodes form reliable and inexpensive connections (col. 1/lis. 35-39 & 49-57). It would have been obvious to one of ordinary skill in the art at the time the invention

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was made to make electrodes disclosed by Terui linking the front and back chip surface and to stack several chips in order to provide a very low cost high density package as taught by Gnadinger because this type of through electrode forms reliable and inexpensive connections

10. Regarding claims 5, 6, and 10, Terui teaches the cross-sectional areas are increased according to a magnitude of an electric current via the through electrodes. For example, Terui teaches that the power supply electrodes 285/287 have a greater sectional area than the signal electrodes 181.

11. Regarding claims 17 and 18, Gnadinger teaches that the cross-sectional areas of those through electrodes which connect $n+1$ or more adjacent semiconductor chips are greater than the cross-sectional areas of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2. Note that each of the electrodes 20 connects multiple adjacent chips 11 (i.e. more than 3) contained in each of the wafers wherein each electrode has lower cross sectional areas that are greater than upper cross sectional areas of another electrode.

Allowable Subject Matter

12. Claims 3, 7, 11, 15, 16, 19, 20, 21, 23, 24, 25, 27 and 28 are allowed.

13. Claims 4, 8, 12, 22, and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

14. Applicant's arguments filed 07/13/2005 have been fully considered but they are not persuasive. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Gnadinger teaches that a very low cost high-density package can be obtained by using this type of through electrodes because this type of electrodes form reliable and inexpensive connections (col. 1/lis. 35-39 & 49-57). In other words, this type of embodiment provides a high-density package since multiple chips can be staked.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonardo Andújar
Patent Examiner
Art Unit 2826
09/25/2005



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